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PATENT APPLICATION
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METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION DUE TO GATE LEAKAGE DURING SLEEP MODE

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BACKGROUND

Field of the Invention

[0001] The present invention relates to the design of CMOS integrated circuits. More specifically, the present invention relates to a method and an apparatus for reducing power consumption due to gate leakage current during sleep mode in CMOS integrated circuits.

Related Art

[0002] Power consumption in complementary metal oxide semiconductor (CMOS) integrated circuits is made up of a dynamic term and a static term. The dynamic term arises from charging and discharging of load capacitances and is proportional to operating frequency. The static term arises from direct current (DC) flow and is independent of operating frequency. In most digital logic

circuits, dynamic power is the dominant term while the chip is active. However, when the clock is stopped and the CMOS device enters a sleep mode to conserve power, static power becomes the dominant term.

[0003] The dominant components of this static power consumption are (1) subthreshold leakage currents from source to drain through transistors that are nominally OFF, and (2) gate leakage currents caused by tunneling of carriers through the very thin gate oxides. FIG. 1A illustrates subthreshold leakage current in a negative channel metal-oxide semiconductor (NMOS) transistor. This leakage current, I_S, flows from the drain (d) to the source (s) when the transistor is off. FIG. 1B illustrates gate leakage current in an NMOS transistor. This current, I_G, flows into the gate due to carriers tunneling across the gate oxide material. In the past, the subthreshold leakage currents have been the dominant component in the static term. However, modern circuits are being built using ever smaller gate thicknesses to improve performance. The effect of these smaller gate thicknesses is to boost the gate leakage term exponentially. FIG. 1C presents a graph illustrating the relative magnitudes of power consumption terms. As shown, dynamic power is increasing gradually with time, while the static power is increasing at a faster rate.

[0004] In many design methodologies, the same underlying design is used for system running off of alternating current (AC) or from batteries. The frequency and power supply voltage are typically reduced to cut dynamic power dissipation in battery-based systems. This will become a problem for future systems because the static power dissipation during the low-power sleep mode may unreasonably limit standby life of system such as laptop computers.

[0005] Several techniques have been suggested to minimize static power dissipation during sleep mode. Most of these techniques have sought to minimize subthreshold leakage, which has traditionally been the largest static power

component. For example, higher threshold devices with less subthreshold leakage may be used, or a body bias may be applied to raise the effective threshold voltage during sleep mode. Unfortunately, these techniques do nothing to reduce gate leakage currents.

[0006] Hence, what is needed is a method and an apparatus to effectively reduce gate leakage current in CMOS integrated circuit devices during sleep mode.

SUMMARY

[0007] One embodiment of the present invention provides a system that achieves low gate leakage current in an integrated circuit during sleep mode. Upon entering sleep mode, the system reduces the power supply voltage applied to the integrated circuit to a low voltage level, wherein the low voltage level is low enough to provide a low gate leakage current, but is high enough to maintain state in the integrated circuit.

[0008] In a variation of this embodiment, the low voltage level is so low that the integrated circuit cannot perform computation operations on data.

[0009] In a variation of this embodiment, the low voltage level is below a threshold voltage for transistors on the integrated circuit.

[0010] In a variation of this embodiment, when the system detects that sleep mode is about to be exited, the system restores the power supply voltage to a nominal operating voltage.

[0011] In a further variation, reducing the power supply voltage involves gradually ramping the power supply voltage to the low voltage level to reduce noise caused by the voltage change.

[0012] In a further variation, restoring the power supply voltage involves gradually ramping the power supply voltage to the nominal operating voltage to reduce noise caused by the voltage change.

[0013] In a further variation, reducing the power supply voltage involves stepping the power supply voltage in discrete steps to the low voltage level to reduce noise caused by the voltage change.

[0014] In a further variation, restoring the power supply voltage involves stepping the power supply voltage in discrete steps to the nominal operating voltage to reduce noise caused by the voltage change.

[0015] In a further variation, the low voltage level is also low enough to provide a low subthreshold leakage in the integrated circuit.

BRIEF DESCRIPTION OF THE FIGURES

[0016] FIG. 1A illustrates subthreshold leakage current in an NMOS transistor.

[0017] FIG. 1B illustrates gate leakage current in an NMOS transistor.

[0018] FIG. 1C presents a graph illustrating the relative magnitudes of static and dynamic power consumption components.

[0019] FIG. 2 presents a graph illustrating gate leakage current density versus applied voltage for several gate thicknesses in accordance with an embodiment of the present invention.

[0020] FIG. 3 presents a graph illustrating the process of ramping the power supply voltage to a low voltage level during sleep mode in accordance with an embodiment of the present invention.

[0021] FIG. 4 presents a graph illustrating the process of stepping the voltage to a low voltage level during sleep mode in accordance with an embodiment of the present invention.

[0022] FIG. 5 illustrates a voltage regulation system in accordance with an embodiment of the present invention.

[0023] FIG. 6 presents a flowchart illustrating the process of reducing power supply voltage during sleep mode and restoring power supply voltage when sleep mode is terminated in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0024] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Power Consumption

[0025] FIG. 2 presents a graph illustrating gate leakage current density versus applied voltage for several gate thicknesses in accordance with an embodiment of the present invention. The arrow indicates predicted scaling of oxide thickness (T_G) and gate voltage (V_G) over various process generations. Note that gate leakage current density (J_G) increases exponentially as gate thickness decreases. Note also that the gate leakage current may be reduced by approximately three orders of magnitude by reducing the gate voltage (V_G) to

approximately 0.3 volts. This voltage level is sufficient to maintain state in a CMOS device while the device is in sleep mode and is not being clocked.

[0026] Most integrated circuit devices receive power from an external voltage regulator. In many systems, this regulator is adjustable. For example, some laptop microprocessors use a higher supply voltage for fast operation when the laptop is plugged into an AC source and a lower supply voltage to conserve dynamic power when operation on a battery. This supply voltage can be further reduced during sleep mode until gate leakage current is at an acceptable level.

Ramping to a Lower Voltage

[0027] FIG. 3 presents a graph illustrating the process of ramping the voltage to a lower level during sleep mode in accordance with an embodiment of the present invention. When the system enters sleep mode, the voltage regulator ramps the voltage to a lower "sleep mode" voltage. Just prior to resuming normal operation, the voltage regulator ramps the voltage up to the nominal voltage for dynamic operation. The rate as which the voltage is ramped up and down can be decided based upon noise tolerance levels for the CMOS circuitry.

Stepping to a Lower Voltage

[0028] FIG. 4 presents a graph illustrating the process of stepping the voltage to a lower level during sleep mode in accordance with an embodiment of the present invention. When the system enters a sleep mode, the voltage regulator steps the voltage in discrete steps to a lower "sleep mode" voltage. Just prior to resuming normal operation, the voltage regulator steps the voltage in discrete steps up to the nominal voltage for dynamic operation. The number and size of the steps can be determined based upon noise tolerance levels for the CMOS circuitry.

Voltage Regulation

[0029] FIG. 5 illustrates a voltage regulation system in accordance with an embodiment of the present invention. This system includes a CMOS integrated circuit 502, a voltage regulator 504, and a power supply 506. Power supply 506 provides DC power for integrated circuit 502 through voltage regulator 504. When voltage regulator 504 receives sleep mode signal 508, voltage regulator reduces the voltage applied to integrated circuit 502 to a low enough level that gate leakage current is reduced, but not so low that integrated circuit 502 cannot maintain state. This low voltage level can, for example, be determined by examining graphs similar to the graph illustrated in FIG. 2. In a variation of this embodiment, voltage is reduced to an even lower level to reduce subthreshold leakage current.

[0030] Subthreshold leakage is exponentially dependent on the drain-source voltage V_{ds} and reaches its full value at a few multiples of the thermal voltage V_t (~25 mV at room temperature). However, this leakage may be reduced by lowering the power supply to a voltage on the order of V_t. At such low voltage levels, care must be taken that noise does not disturb the system state.

[0031] When sleep mode signal 508 is removed prior to resuming normal operation, voltage regulator 504 returns the voltage to the nominal operating level. Note that voltage regulator 504 can either ramp the voltage or step the voltage between the different levels.

Reducing Power Consumption

[0032] FIG. 6 presents a flowchart illustrating the process of reducing power supply voltage during sleep mode and restoring the voltage when sleep mode is terminated in accordance with an embodiment of the present invention. The system starts when a signal is detected indicating that the system is going into

sleep mode (step 602). Next, the system signals the voltage regulator to reduce the voltage applied to the system's integrated circuits (step 604). In response, the voltage regulator reduces the voltage as described above in conjunction with FIG. 5. The system then waits for a signal that sleep mode is about to complete (step 606).

[0033] Upon receiving the signal that sleep mode is about to complete, the system restores the voltage to the system's integrated circuits to a nominal value for operation (step 608). Finally, the system leaves sleep mode and continues normal operation (step 610).

[0034] The foregoing descriptions of embodiments of the present invention have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. The scope of the present invention is defined by the appended claims.